CLAIMS

What is claimed is:

1. In a system that asserts a false synchronization signal at times when data is not present, a transponder that produces a lock signal only when data is present, the transponder comprising:

an output adapted to couple to a host device;

a controller chip that includes a phase locked loop adapted to operate in a hunting mode and a locked mode, wherein the phase locked loop asserts a synchronization signal in the hunting mode when a hunting frequency passes through a data signal frequency and wherein the phase locked loop keeps the synchronization signal asserted as long as the phase locked loop is locked onto a data signal; and

a timing circuit that measures a period of time that the synchronization signal is asserted and produces a lock signal if the synchronization signal is asserted for a least a specified period of time.

2. The transponder of claim 1, wherein the timing circuit is an analog timer comprising a capacitor and a resistor network.

3. The transponder of claim 2, wherein the timing circuit comprises a transistor for resetting the timing circuit.

4. The transponder of claim 3, wherein the transistor is at least one of a PNP and NPN bipolar junction transistor.

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5. The transponder of claim 3, wherein the transistor is a field effect transistor.

6. The transponder of claim 1, further comprising an input level detector that compares the synchronization signal with a reference signal and produces logical signals that may be fed into the timing circuit.

7. The transponder of claim 2, the timing circuit further comprising a comparator that receives a signal from the capacitor and resistor network and a reference signal as input and that outputs the lock signal to the host device based on the value of the reference signal compared to the signal from the capacitor and resistor network.

8. The transponder of claim 7, wherein the comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value.

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9. A fiber-optic transponder comprising:

an output adapted to couple to a host device;

a controller chip having includes a phase locked loop that is adapted to operate in a hunting mode that briefly asserts a synchronization signal when a hunting frequency passes through a data signal frequency and that is adapted to operate in a locked mode that asserts the synchronization signal so long as the phase locked loop is locked onto a data signal; and

a translation circuit that converts the synchronization signals from the controller chip to a lock signal usable by the host device, wherein a logic level of the lock signal is asserted when the phase locked loop is locked onto a data signal and is de-asserted when the controller asserts the synchronization signal in hunting mode.

10. The fiber-optic transponder of claim 9, the translation circuit comprising a timer that measures a period of time that the synchronization signal is asserted.

11. The fiber-optic transponder of claim 10, the translation circuit comprising an input level detector that acts as a comparator to the synchronization signal and a reference signal and that produces logical signals usable by the translation circuit to determine when the synchronization signal is asserted because the phase locked loop is locked onto a data signal and when the synchronization signal is asserted because a hunting frequency passes through a data signal frequency in hunting mode.

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12. The fiber-optic transponder of claim 9, the translation circuit further comprising a comparator, wherein the comparator receives as an input a signal from the timer and a reference signal and outputs the lock signal for use by the host device based on a comparison of the signal from the timer and the reference signal.

13. The fiber-optic transponder of claim 12, wherein the comparator includes feedback that changes a logical level of the lock signal when the value of the lock signal changes by some value greater than a hysteresis threshold value.

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14. A method of mediating signals from a controller chip used in a fiber-optic transponder with a host device in order to control a logic level of a lock signal used by the host device, the method comprising:

receiving an asserted synchronization signal from a phase locked loop, the phase locked loop disposed on the controller chip;

determining whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency; and

asserting a lock signal if the phase locked loop has locked onto a data signal.

15. The method of claim 14, wherein determining whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency further comprises:

measuring a period of time that the synchronization signal is asserted; and

determining that the synchronization signal is caused by the phase locked loop locking onto the data signal if the period of time that the synchronization signal is asserted is greater than a specified period of time.

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16. The method of claim 14, further comprising comparing the asserted synchronization signal with a reference signal to determine if the asserted synchronization signal is produced by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through the data signal frequency.

17. The method of claim 14, further comprising comparing the lock signal with a reference signal to produce the lock signal useful by a host device coupled to the fiber-optic transponder.

18. The method of claim 14, further comprising changing a logical level of the lock signal when the value of the lock signal changes by some value greater than a hysteresis threshold value.

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19. In a system that generates a synchronization signal to indicate the presence of a data signal, wherein the synchronization signal may be asserted when the data signal is not present, a translation circuit that receives the synchronization signal and asserts a lock signal only when a data signal is present and that does not assert the lock signal when the data signal is not present, the translation circuit comprising:

a timing circuit that measures a period of time that the synchronization signal is asserted using at least a capacitor, wherein the timing circuit generates an output signal having a voltage across the capacitor; and

a comparator circuit that compares the output signal with a reference signal such that a lock signal is asserted based on the comparison of the output signal with the reference signal.

20. The translation circuit of claim 19, wherein the timing circuit comprises a transistor that is controlled by the synchronization signal for resetting the timing circuit such that the capacitor discharges.

21. The translation circuit of claim 20, wherein the transistor is at least one of a PNP bipolar junction transistor, an NPN bipolar junction transistor, and a field effect transistor.

22. The translation circuit of claim 19, wherein the comparator circuit includes feedback that changes a logical level of the lock signal useful by the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value of the comparator circuit.

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23. The translation circuit of claim 22, wherein the hysteresis threshold value of the comparator circuit prevents the lock signal from changing logic levels until the output signal of the timing circuit changes by an amount greater than the hysteresis threshold value.

24. The translation circuit of claim 22, further comprising an input level detector that passes the synchronization signal to the timing circuit when the synchronization signal exceeds a reference voltage.

25. The translation circuit of claim 22 wherein the capacitor charges slowly and discharges quickly and wherein the comparator circuit asserts a lock signal when the voltage across the capacitor exceeds the reference signal.

26. The translation circuit of claim 22 wherein the capacitor charges quickly and discharges slowly and wherein the comparator asserts a lock signal when the reference signal exceeds the voltage across the capacitor.

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